AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Page 10, the last paragraph, which bridges to page 11:

Clock signal receiving circuit 32 comprises second reference voltage generating circuit 4 and second comparator 5. Second reference voltage generating circuit 4 receives second control signal 15 which is supplied from controlling circuit 1 in clock signal transmitting circuit 31 through ~~ransmission~~transmission path 33, determines second reference voltage 17 corresponding to second control signal 15, and outputs second reference voltage 17. Second comparator 5 inputs transmission clock signal 12 which is supplied from clock signal transmitting circuit 31 through transmission path 33 and whose frequency periodically varies and second reference voltage 17 which is generated in second reference voltage generating circuit 4, compares transmission clock signal 12 with second reference voltage 17, and outputs reproduced clock signal 13 having a single frequency.

Page 12, the last paragraph, which bridges to page 13:

Next, the operation of first comparator 3 will be explained. At the beginning, first reference voltage generating circuit 2 selects VT1 as first reference voltage 16 corresponding to first control signal 14. When the voltage source clock signal 11 becomes VT1 (waveform 101) at time T21, first comparator 3 determines that the logical level of source clock signal 11 becomes high and causes the logical level (waveform 102) of transmission clock signal 12 to be high. After first reference voltage generating circuit 2 causes the voltage level of first reference voltage 16 to be raised to VT2., when the voltage level of source clock signal 11 becomes VT2 at

time T22, first comparator 3 causes the logical level (waveform 102) of transmission clock signal 12 to be low. Thereafter, because first reference voltage generating circuit 2 varies the voltage level of first reference voltage 16 as represented by waveform 104, first comparator 4 outputs transmission clock signal 12 are represented by waveform 102. It is apparent that frequency of transmission clock signal 12 (waveform 102) periodically varies. The change amount and change period of the frequency of transmission clock signal 12 depend on the period of source clock signal 11 and the resolution of first reference voltage 16.

Page 16, the first full paragraph:

As the relation of the first reference voltage of clock signal transmitting circuit 31 and the second reference voltage of ~~tclock~~clock signal receiving circuit 32, VT1 corresponds to VT15; VT2 corresponds to VT14; VT3 corresponds to VT13; VT4 corresponds to VT12; and VT5 corresponds to VT11. In other words, he lowest voltage level of first reference voltage 16 of clock signal transmitting circuit 31 corresponds to the highest voltage level of second reference voltage 17 of clock signal receiving circuit 32. The second lowest voltage level of first reference voltage 16 corresponds to the second highest voltage level of second reference voltage 17. The rest of the voltage levels satisfy the same relation. This the relation of VT1 + VT15 = VT2 + VT14 = VT3 + VT13 = VT4 + VT12 = VT5 + VT11 = (a constant voltage) is satisfied. The voltage level of second reference voltage 17 varies in the order of VT15, VT14, VT13, VT12, VT11, VT12, VT13, VT14, VT15, VT14, VT13, and so forth when the logical level of source clock signal 11 changes.